L7029B Small Outline ADPCM CODEC

Table of Contents

L7029B ADPCM CODEC

1. GENERAL DESCRIPTION

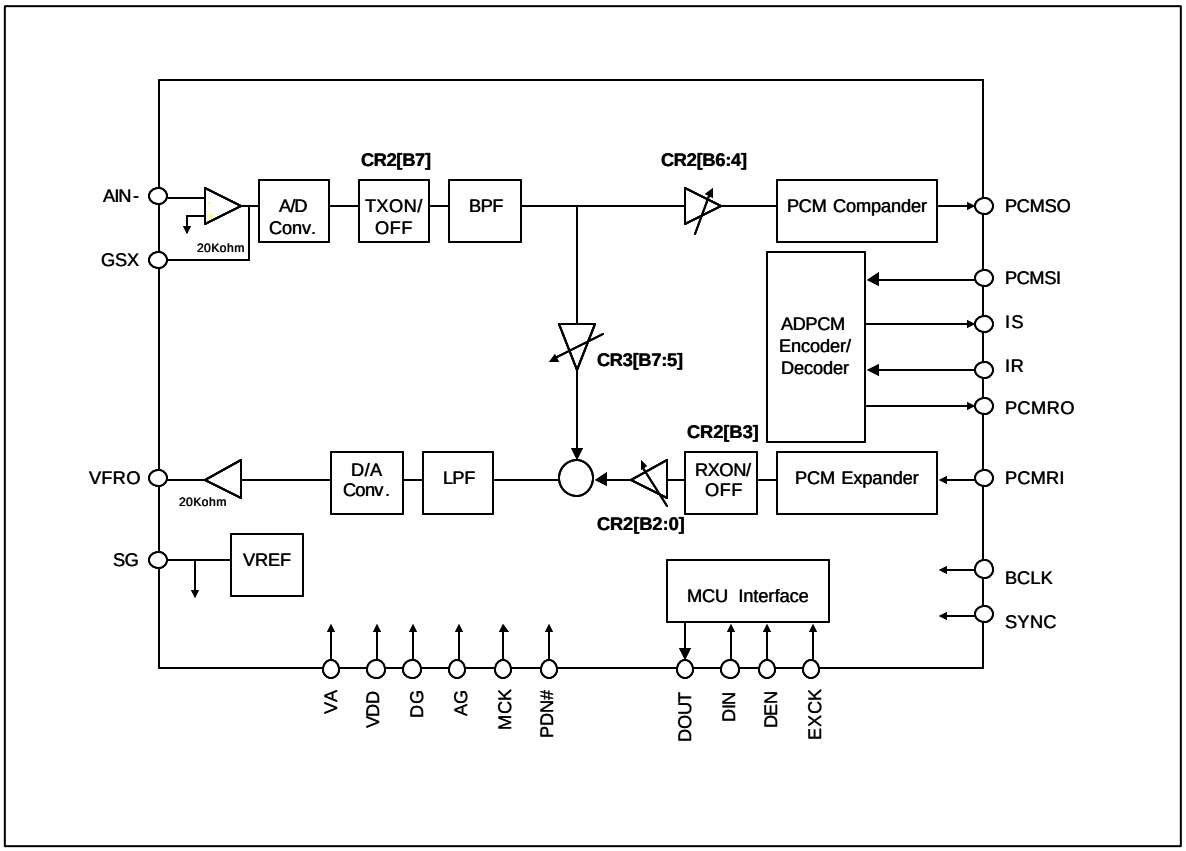
The Lanwave L7029B ADPCM Codec is a single channel device which performs mutual transcoding between the analog voice band signal and 32kbps ADPCM serial data.

This chip allows full-duplex operation over a voltage range from 2.7 to 3.6 volts; it's extremely low power consumption makes it ideal for battery or AC powered applications. The chip includes a serial MCU setup port interface with a simple 4-byte setup and status register set. A microcontroller can access built-in features through the MCU interface. In addition, this chip also consists of some analog OP amps integrated with a ΣΔ PCM codec-filter to allow for easy control of the analog interface. It has a built in transmit band pass filter to suppress residual RF noise pickup through the microphone port.

This chip can be used in conjuction with any other Lanwave SATURN family of base band CD/SS™ DSP devices to perform voice communication functions with a minimum amount of external discrete electronic components.

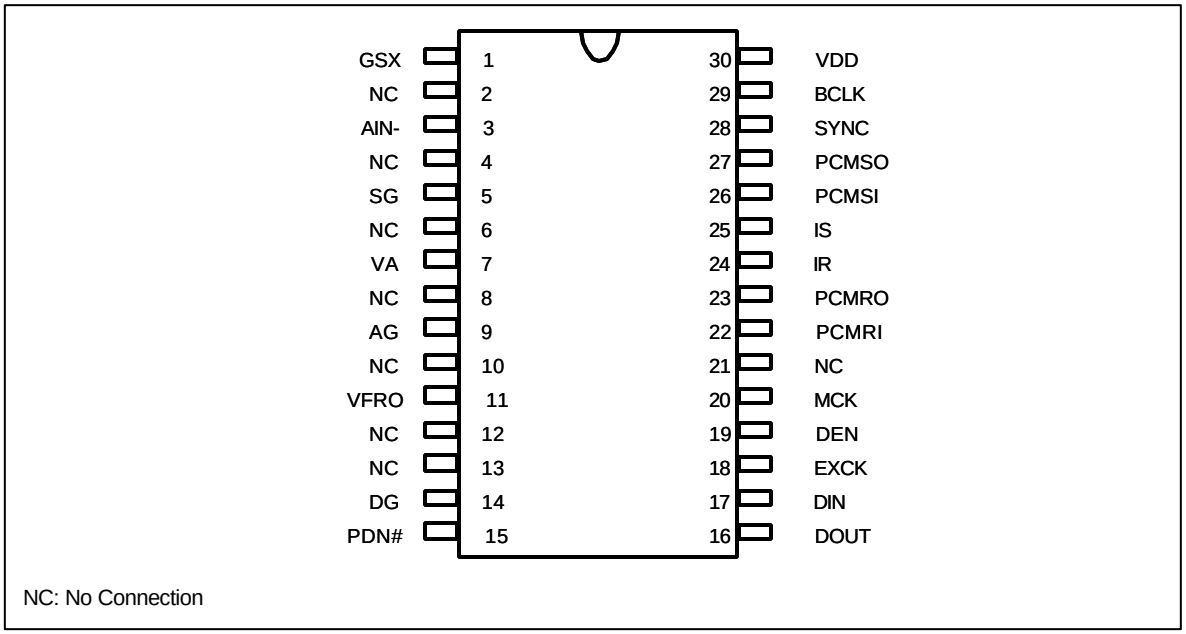
2. FEATURES

- Single 2.7 to 3.6 volt power supply
- Master clock rate: 10.368 MHz
- Typical power consumption of 6mA, or 18 mW for 3 volt; power down to 0.01mA, or 0.03 mW
- Full-duplex single channel Transmit / Receive operation
- Linear 14 bit ΣΔ PCM codec-filter for A/D and D/A converter
- Integrated transmit band pass filter eliminating RF residual TDD noise
- Mu-Law voice companding (u-Law) for the best sound quality.
- ADPCM transcoder for 32 kbps bit rate. (Compliant with ITU-T G.726)
- Serial PCM/ADPCM transfer data rate from 64 kbps to 2048 kbps
- Sampling frequency: 8 kHz typical.
- Programmable transmit gain, receive attenuation, and sidetone attenuation (8-Step adjustment)
- 4 Setup and status byte registers for monitoring
- Housed in 30-pin plastic SSOP space saving package



BLOCK DIAGRAM

3. PIN CONFIGURATION



NC: No Connection

30-Pin Plastic SSOP

4. PIN DESCRIPTIONS

4.1. Power Control Interface

PIN NAME	PIN NO.	I/O	FUNCTION
VDD	30	I	Digital +3V power supply. This power supply is separated from the analog signal power supply pin (VA). The VDD pin must be kept as close as possible to VA on the PCB.
VA	7	I	Analog +3V power supply.
DG	14	I/O	Digital ground. This ground is separated from the analog signal ground pin (AG). The DG pin must be kept as close as possible to AG on the PCB.
AG	9	I/O	Analog ground.
SG	5	I/O	Analog signal ground. The output voltage of this pin is approximately 1.4Volt. Put 10uF plus 0.1uF (ceramic type) bypass capacitors between this pin and AG. During power-down, this output voltage is 0 Volt. This pin should be used via a buffer if used externally.

4.2. Analog Interface

PIN NAME	PIN NO.	I/O	FUNCTION
GSX	1	O	Transmit level adjustment. GSX is connected to the transmit amplifier output. During power-down mode, the GSX output is a high impedance state.
AIN-	3	I	Transmit analog input. AIN- is connected to the inverting input of the transmit amplifier.
VFRO	11	O	Receive analog output. During power-down mode, the VFRO output is in a high impedance state.

4.3. ADPCM/PCM Serial Interface

PIN NAME	PIN NO.	I/O	FUNCTION
MCK	20	I	Master clock input. The frequency is 10.368MHz typical. The master clock signal may be asynchronous with BCLK and SYNC.
PCMSO	27	O	Transmit PCM data output. PCM is output from MSB in synchronization with the rising edge of BCLK and SYNC. Refer to Figure 1. During power-down, the PCMSO output is at “Low” level.
PCMSI	26	I	Transmit PCM data input. This signal is converted to the transmit ADPCM data, PCM is shifted in synchronization with the falling edge of BLCK. Normally, this pin is connected to PCMSO. Refer to Figure 1.
PCMRO	23	O	Receive PCM data output. PCMRO is the output signal after ADPCM decoder processing. This signal is output serially from MSB in synchronization with the rising edge of BCLK and SYNC. Refer to Figure 1. During power-down, the PCMRO output is at “Low” level.
PCMRI	22	I	Receive PCM data input. PCMRI is shifted on the rising edge of BCLK and input from MSB. Normally, this pin is connected to PCMRO. Refer to Figure 1.
IS	25	O	Transmit ADPCM signal output. After having encoded PCMSI with ADPCM, the signal is output from MSB in synchronization with the rising edge of BCLK and SYNC. Refer to Figure 1. This pin is at “HIGH” level during power-down.
IR	24	I	Receive ADPCM signal input. This input signal is shifted serially on the falling edge of BCLK and SYNC and input from MSB. Refer to Figure 1.
BCLK	29	I	Shift clock input for the PCM and ADPCM data. The frequency is set in the range of 8 to 256 times the SYNC frequency. Refer to Figure 1.
SYNC	28	I	Sampling input for the PCM and ADPCM data. The frequency is 8kHz. Synchronize this signal with BCLK signal. SYNC is used to indicate the MSB of the PCM data stream. Refer to Figure 1.

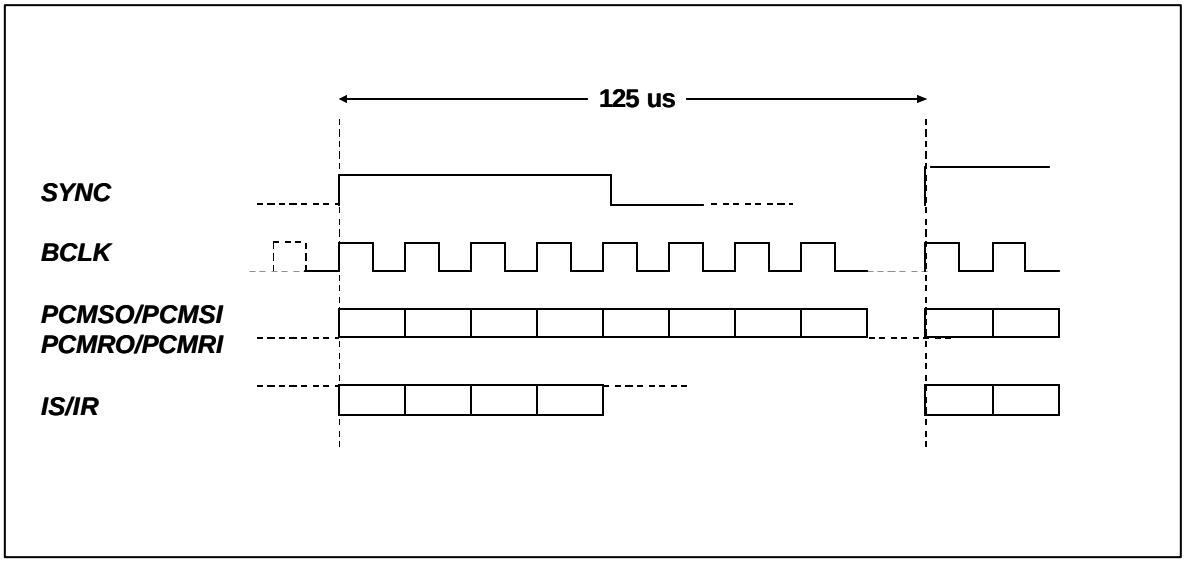
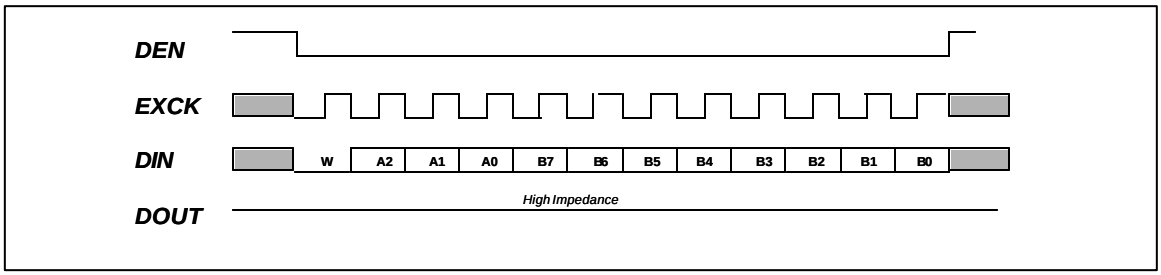


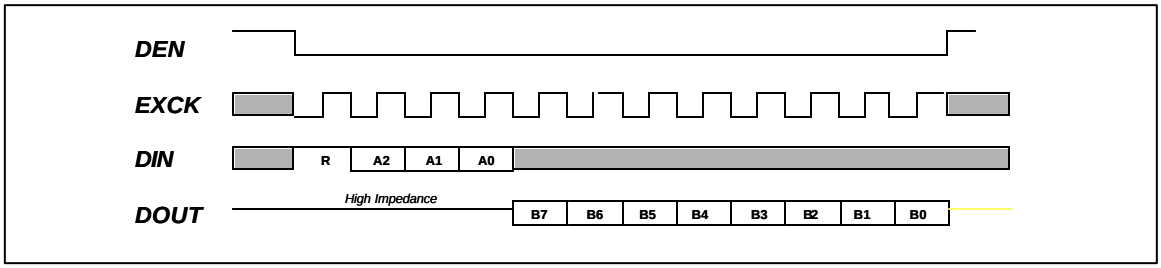
Figure 1. PCM and ADPCM Interface Basic Timing.

4.4 Serial Control Port Interface

PIN NAME	PIN NO.	I/O	FUNCTION
PDN#	15	I	Power-down and reset control input. A “LOW” level makes the IC enter a power-down state. At the same time, all control register data are reset to the initial state. Set this pin to “HIGH” during normal operating mode. The power-down state is controlled by a logical OR with CR0[bit5] of the control register. When using PDN# for power-down and reset control, set CR0[5] to digital “0”. The reset width (a “LOW” level period) should be 200ns or more. Be sure to reset the control registers by executing this power down to keep this pin to digital “0” level for 200ns or longer after the power is turned on and VDD exceeds 2.7V.
DEN	19	I	DEN is the ENABLE control signal input. This and the following pins is controlled by an external MCU to read and write data into the L7029B internal registers.
EXCK	18	I	EXCK is the data shift clock input.
DIN	17	I	DIN is the address and data input.
DOUT	16	O	DOUT is the data output. During power-down, the DOUT output is in a high impedance state.

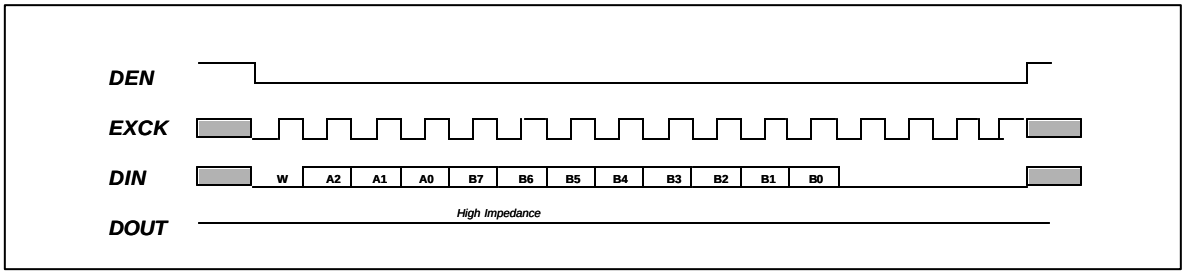


(a) Data Write Timing Diagram

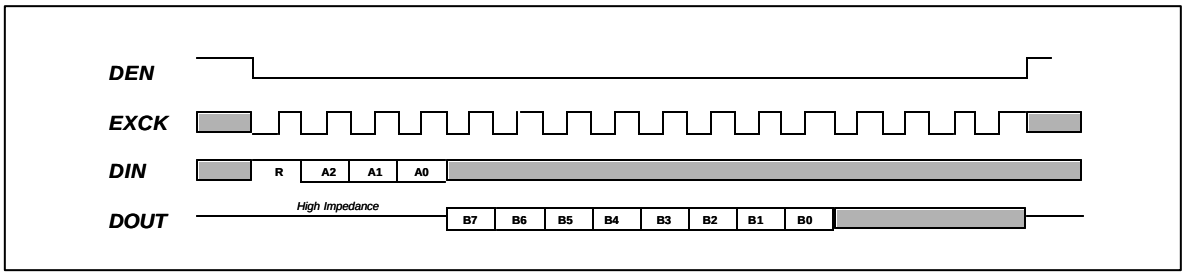


(b) Data Read Timing Diagram

Figure 2-1. MCU Interface Input/Output Timing (DIN = 12bits)



(a) Data Write Timing Diagram



(b) Data Read Timing Diagram

Figure 2-2. MCU Interface Input/Output Timing (DIN = 16 bits)

5. CONTROL AND STATUS REGISTERS MAP

	A2	A1	A0	B7	B6	B5	B4	B3	B2	B1	B0	
CR0	0	0	0	--	--	PDN ALL	--	--	--	--	--	R/W
CR1	0	0	1	TEST0	TEST1	TX RESET	RX RESET	TX MUTE	RX MUTE	--	RX PAD	R/W
CR2	0	1	0	TX ON/OFF	TX GAIN2	TX GAIN1	TX GAIN0	RX ON/OFF	RX GAIN2	RX GAIN1	RX GAIN0	R/W
CR3	0	1	1	Side Tone GAIN2	Side Tone GAIN1	Side Tone GAIN0	--	--	--	TEST2	TEST3	R/W

R/W: Readable/Writable.

5.1 CR0 (Basic operating mode setting) Initial value = xx0x xxxx

	B7	B6	B5	B4	B3	B2	B1	B0
CR0	-	-	PDN ALL	-	-	-	-	-

B7, B6, B4 to B0: Not used. (These pins are used to test the device. They should be set to “0” during normal operation.)

B5: Power-down (entire system); 0/Power-on, 1/Power-down
“OR”ed with the inverted external power-down signals.
When using this register, set the PDN# pin to “1”.

5.2 CR1 (ADPCM operating mode setting) Initial value = 0000 00x0

	B7	B6	B5	B4	B3	B2	B1	B0
CR1	TEST0	TEST1	TX RESET	RX RESET	TX MUTE	RX MUTE	--	RX PAD

B7, B6: Test bit for L7029B. Set to “0” during normal operation.

B5: Reset of transmit ADPCM (specified by G.726); 1/Reset*

B4: Reset of receive ADPCM (specified by G.726); 1/Reset*

B3: ADPCM transmit data mute; 1/Mute

B2: ADPCM receive data mute; 1/Mute

B1: Not used. Set to "0" during normal operation.

B0: Receive side PAD; 1/inserted 12dB loss in the receive side voice Path.
0/no PAD

* The reset width should be 1/fsample microseconds or more.

The transmit and receive sides cannot be reset separately, and must be reset at the same time.

5.3 CR2 (Operating mode setting and gain adjustment) Initial value = 0011 0011

	B7	B6	B5	B4	B3	B2	B1	B0
CR2	TX ON/OFF	TX GAIN2	TX GAIN1	TX GAIN0	RX ON/OFF	RX GAIN2	RX GAIN1	RX GAIN0

B7: Transmit PCM signal ON/OFF; 0/ON, 1/OFF

B6, B5, B4: Transmit signal gain adjustment, refer to table below.

B3: Receive PCM signal ON/OFF; 0/ON, 1/OFF

B2, B1, B0: Receive signal gain adjustment, refer to table below.

B6	B5	B4	Transmit Gain	B2	B1	B0	Receive Gain
0	0	0	-6dB	0	0	0	-6dB
0	0	1	-4dB	0	0	1	-4dB
0	1	0	-2dB	0	1	0	-2dB
0	1	1	0dB	0	1	1	0dB
1	0	0	+2dB	1	0	0	+2dB
1	0	1	+4dB	1	0	1	+4dB
1	1	0	+6dB	1	1	0	+6dB
1	1	1	+8dB	1	1	1	+8dB

5.4 CR3 (Side tone gain setting) Initial value = 000x xx00

	B7	B6	B5	B4	B3	B2	B1	B0
CR3	Side Tone GAIN2	Side Tone GAIN1	Side Tone GAIN0	--	--	--	TEST2	TEST3

B7, B6, B5: Side tone path gain adjustment, refer to table below.

B4 to B2: Not used. (These should be set to “0” during normal operation.)

B1, B0: Test bits for L7029B. (These should be set to “0” during normal operation.)

B7	B6	B5	Side Tone Path Gain
0	0	0	OFF
0	0	1	-21dB
0	1	0	-19dB
0	1	1	-17dB
1	0	0	-15dB
1	0	1	-13dB
1	1	0	-11dB
1	1	1	-9dB

6. ELECTRICAL CHARACTERISTICS

6.1. Absolute Maximum Ratings

(Voltage Referenced to DG pin)

PARAMETER	SYMBOL	RATING	UNIT
Power Supply Voltage	VEXT, VDD	-0.3 to +5.0	V
Analog Input/Output Voltage	V_{AIN}	-0.3 to VDD + 0.3	V
Digital Input/Output Voltage	V_{DIN}	-0.3 to VEXT + 0.3	V
Operating Temperature	TOP	-25 to +85	¢J
Storage Temperature	TSTG	-55 to +150	¢J

Note: Exposure to conditions beyond those listed under Absolute Maximum Ratings may adversely affect the life and reliability of the device.

6.2. DC Characteristics

(VSS = 0 volt TOP = -25 to +85° C)

PARAMETER	SYM.	CONDITION	MIN.	TYP.	MAX.	UNIT
Operating Voltage	VDD	Must be fixed	+2.7	3.0	+3.6	V
Operating Current	IEXT	MCLK = 10.368 MHz, Operating mode, no signal	---	6.0	---	mA
Power Down Current	IPWDN	MCLK Off	---	0.01	0.1	mA
Input High Voltage	VIH	All digital input pins	0.45xVDD	---	VDD	V
Input Low Voltage	VIL	All digital input pins	0	----	0.16x VDD	V
Output High Voltage	VOH	IOH = 4mA	2.1	----	-----	V
Output Low Voltage	VOL	IOL = -4mA	0	---	0.4	V
Input High Current	IIL	VI = 0V	---	---	0.5	uA
Input Low Current	IIH	VI = VDD	---	---	+2	uA
Input Capacitance	CIN		---	5	---	pF
Master Clock Freq	FMCK	MCK	---	10.368	---	MHz
Master Clock Accuracy		MCK	-0.01%	SYNC x 1296	+0.01 %	MHz
BCLK duty	FBCK	BCLK	SYNC x 8	---	SYNC x 256	KHz
Sampling Frequency		SYNC	---	8.0	---	kHz

MCK duty ratio		MCK	30	50	70	%
Clock duty ratio		BCLK, EXCK	30	50	70	%
Digital input rise time	Tir	Digital input pins	---	---	50	ns
Digital input fall time	Tif	Digital input pins	---	---	50	ns
PCM Sync Signal Settling time (Continuous clock)	TBS	BCLK <-> SYNC	100	---	---	ns
PCM Sync Signal Settling time (Burst Mode clock)	TSB	BCLK <-> SYNC	0	---	20	us
SYNC signal width (Continuous BCLK)	TWS	SYNC	1BCLK	---	(SYNC minus 1) BCLK	us
SYNC signal width (Burst Mode clock)	TWSB	SYNC	1BCLK	---	Burst Clock minus 1	us
PCM, ADPCM setup time	Ts	---	100	---	---	ns
PCM, ADPCM hold time	Th	---	100	---	---	ns
Digital output load	CDL	Digital output pins	---	---	100	pF
Bypass Capacitor for SG	CSG	SG to AG	10+0.1	---	---	uF

6.3. Analog Transmission Characteristics

(VDD = +2.7 to 3.6V, DG = 0 volt , Top = -25 to +85° C ; all analog signal referenced to SG; MCLK = 10.368MHz ; Unless otherwise noted)

6.3.1. Amplitude Response for Analog Transmission Performance

PARAMETER	SYM.	CONDITION	TYP.	TRANSMIT		RECEIVE		UNIT
				MIN.	MAX.	MIN.	MAX.	
Absolute Level	A_{VR},A_{VT}	1020 Hz (VFRO, GSX)	0.320	0.285	0.359	0.285	0.359	Vrms
Frequency Response, Relative to 0 dbm0 @ 1020Hz	GRTV	60 Hz	0	30	--	--	--	dB
		300 Hz		-0.5	1.5	-0.5	0.5	
		1050 Hz		Ref	Ref	Ref	Ref	
		3400 Hz		-0.5	1.0	-0.5	1.0	
		3970 Hz		12	--	--	--	

Idle Channel Noise		PCMRI = 11111111	AIN- = SG	--	-68	--	-72	dBm0 pP
Gain Accuracy	DG	All stages, to programmed value	0	-1.0	+1.0	-1.0	+1.0	dB
Transmit & Receive S/N ratio		Freq = 1020 Hz	3	35	---	35	---	dB

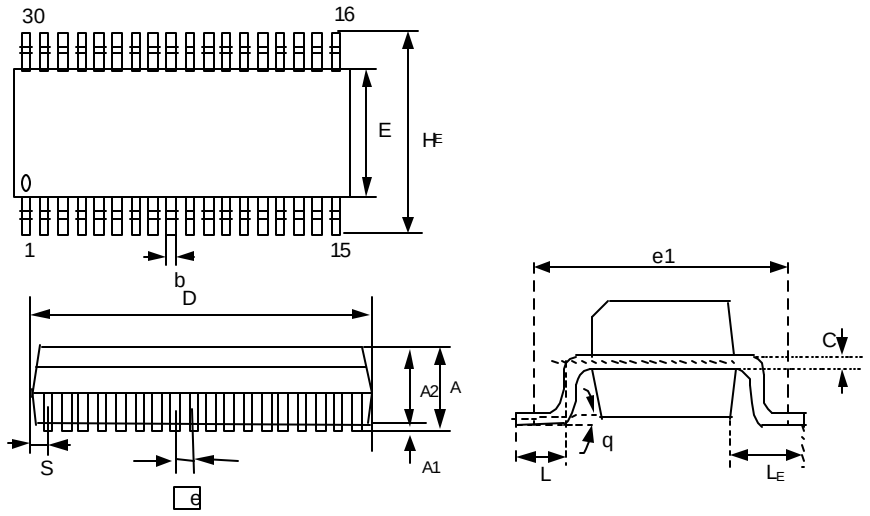
* 0.320Vrms = 0 dBm.

6.4. Digital Switching Characteristics

(V_{EXT} = +2.7 to 3.6V ; DG = 0V; all digital circuits referenced to DG; Top = -25 to +85° C, C_L = 50 pF)

PARAMETER	SYM.	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Digital Input Settling time		All digital input pins	---	---	200	nS
Digital Output Settling time		All digital input pins	---	---	200	nS
Transmit Sync. Timing	T_{XS}	BCLKT to SYNC	50	---	---	nS
	T_{SX}	SYNC to BCLKT	50	---	---	nS
Receive Sync. Timing	T_{RS}	BCLKT to SYNC	50	---	---	nS
	T_{SR}	SYNC to BCLKT	50	---	---	ns
Setup Time for IS Valid	T_{STDR}	---	50	---	---	nS
Hold Time for IR Valid	T_{HDDR}	---	50	---	---	nS
Output Delay Time for IS Valid	T_{DV}	BCLKT to IS	50	---	50	nS
Output Delay Time for IS High Impedance	T_{DHI}	BCLKT to IS	50	---	50	nS

7. PACKAGE DIMENSIONS



30-pin Plastic SSOP Package

SYMBOL	DIMENSION IN MM
A	1.85 Max.
A1	0 ~ 0.25
A2	1.5 ±0.2
b	0.24 +0.08 -0.07
e	0.65 typical
D	9.7±0.1
E	5.6 ±0.1
HE	7.6 ±0.2
L	0.5 typ., 0.6 ± 0.2
LE	1.0 ± 0.2
C	0.17 ±0.05
S	0.3 typical
q /θ	0–10 degree

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